AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 5, line 9 with the following amended paragraph:

Each of the bit line pairs of the memory array 140 may be enabled by one of a plurality of column select circuits 160 (or column selectors). Only one column select circuit 160 is labeled in FIG. [[3]] 2 for ease of illustration. Each column select circuit may simultaneously connect one of every eight bit line pairs b_{0-7} to the corresponding SA.

Please replace the two paragraphs beginning on page 8, line 14 with the following amended paragraphs:

The SRAM cell 300 also includes an NMOS transistor 340 having a ~~source~~ drain coupled to a body (i.e., an n-well) of each of the transistors 302 and 312 to apply a forward body bias based on the mode or state of the SRAM device (or based on the mode or state of the cell). The mode (such as ACTIVE or INACTIVE/STANDBY) may be determined and/or controlled by the power control device 27 based on the overall memory (or portions of the memory). A ~~drain~~ source of the transistor 340 is coupled to GROUND, and a gate of the transistor 340 is coupled to a signal line 345 that receives a signal representing a state or mode of the memory (such as a STANDBY mode) or portions of the memory, for example. The transistor 340 may operate so as to apply a forward body bias to the PMOS transistors 302 and 312 during a STANDBY mode in which the supply voltage VCC to the cache (i.e., the SRAM device) is also lowered for power savings. For example, in a STANDBY mode, the power control device 27 (shown in FIG. 1) may output a signal representing a STANDBY mode. This signal may be received at the gate of the transistor

340 along the signal line 345. This signal turns ON the transistor 340 so as to apply the forward body bias to both the transistors 302 and 312. The power control device 27 may also appropriately lower the supply voltage VCC applied to the SRAM device (such as on the signal line 310) to a supply voltage of VCCmin. This may result in greater power savings.

Applying the forward body bias makes the PMOS transistors 302 and 312 stronger because of a lower threshold voltage Vt through the body effect. As a result, the inverter characteristics are less skewed towards the NMOS side (as shown in FIG. 4) and the minimum supply voltage VCCmin is lowered thereby allowing greater power savings. Embodiments of the present invention may avoid requiring a separate body bias generator for each of the PMOS transistors 302 and 312 since the n-wells of the PMOS transistors 302 and 312, which form the PMOS bodies, are shorted to GROUND through the NMOS transistor 340 when the transistor 340 is turned ON.